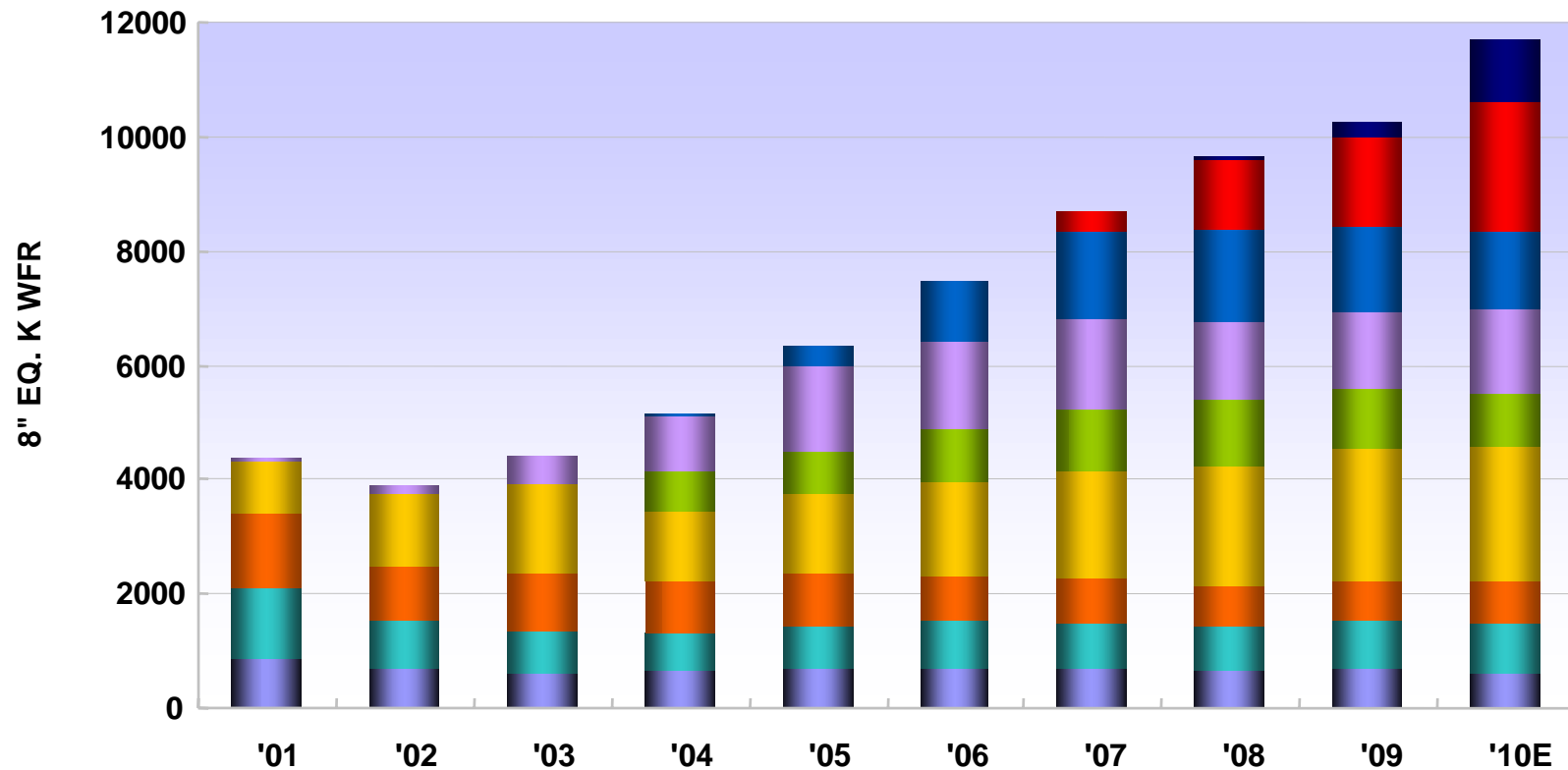


EUV Lithography for Sub-20-nm Semiconductor Manufacturing

Anthony Yen

Taiwan Semiconductor Manufacturing Company

TSMC Installed Capacity by Technology Nodes



0.5um+ 0.35um 0.25um 0.18um 0.15um 0.13um 90nm 65nm 40nm

TSMC to Continue Capacity Expansion



Fab12 Phase 5
Tool move-in 3Q '10



Fab12 Phase 6
Secured land

Fab12



Fab14 Phase 4
Tool move-in 1Q '11

Fab14

**Three
GigaFabs™
under
construction**

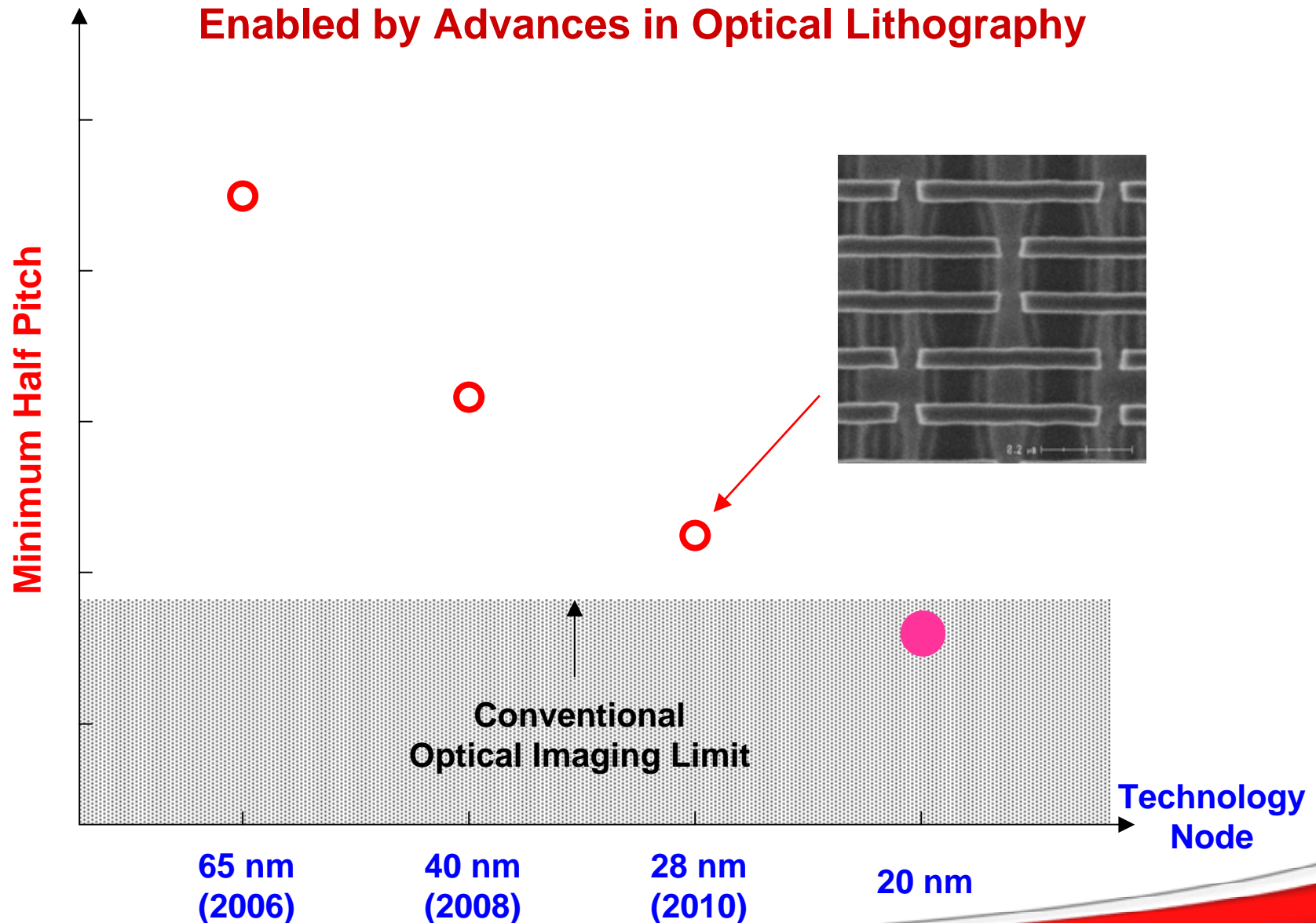


Fab15 Phase 1
Tool move-in 2Q '11

Fab15

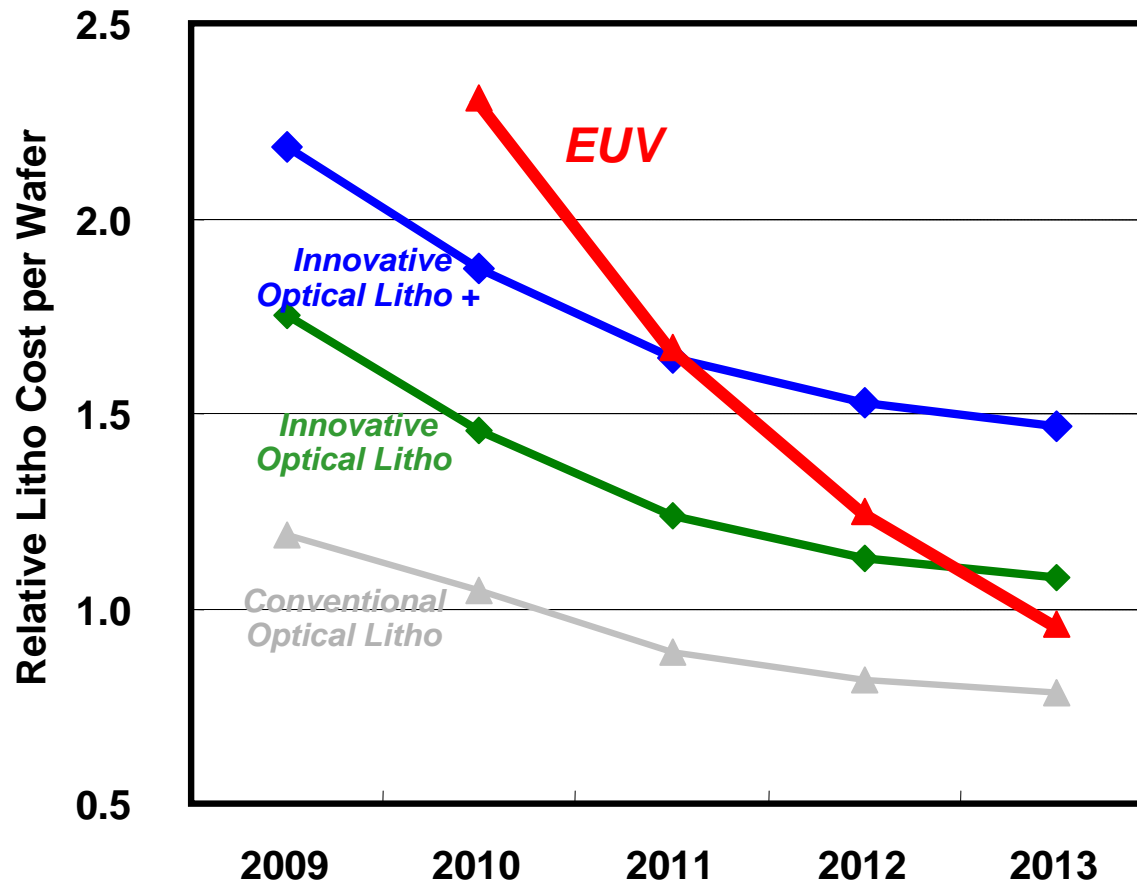
TSMC Technology Roadmap

Enabled by Advances in Optical Lithography



EUVL Will Have a Cost Advantage

if suppliers execute to their throughput roadmaps

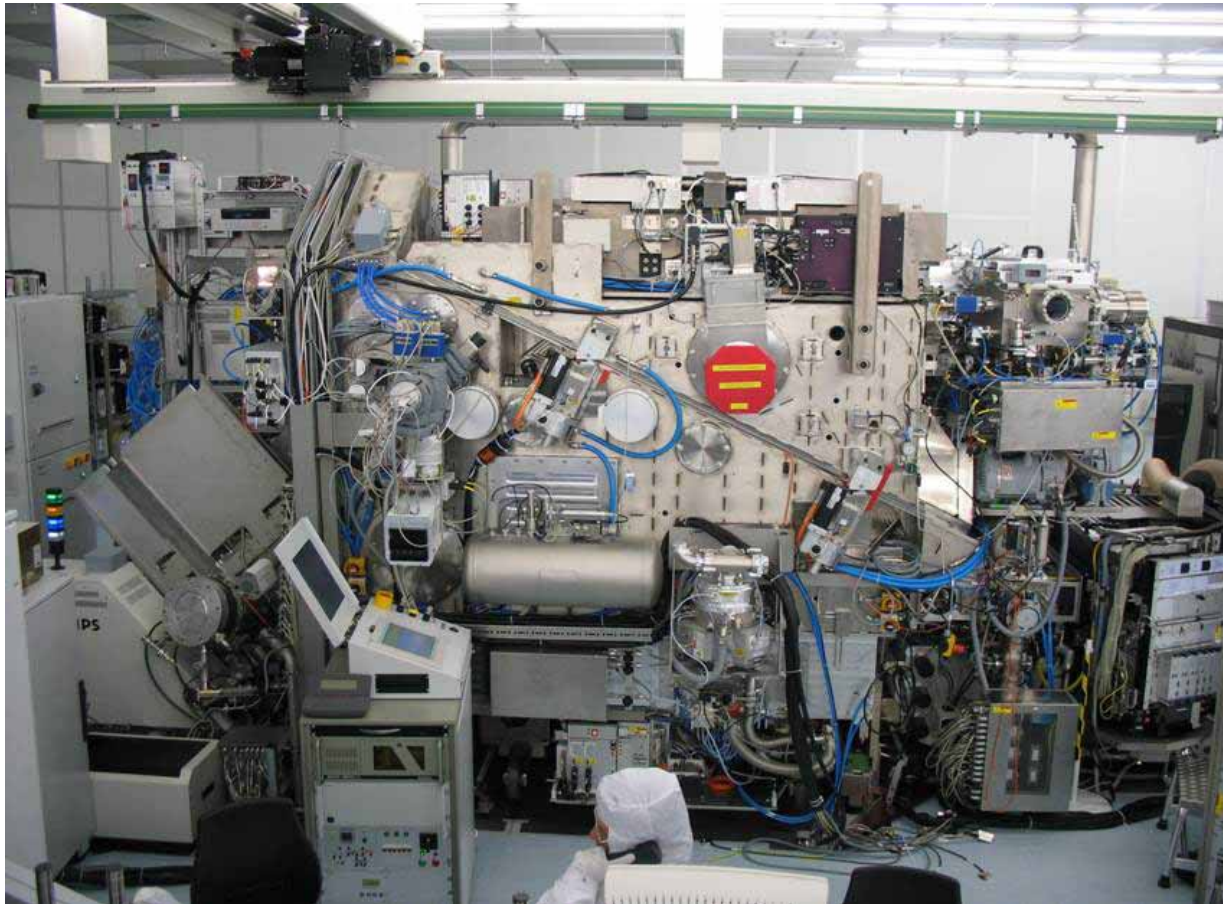


TSMC Will Develop EUV Lithography for Future Technology Nodes

- **Veldhoven, the Netherlands and Hsinchu, Taiwan, R.O.C.
— February 22, 2010 —**
 - **ASML Holding NV (ASML) today announced that Taiwan Semiconductor Manufacturing Company (TWSE: 2330, NYSE: TSM) will take delivery of a TWINSCAN NXE:3100 extreme ultra-violet (EUV) lithography system. This tool represents one of six NXE:3100 EUV systems for ASML's worldwide partners and customers.**
 - **TSMC is expected to be the first dedicated foundry conducting on-site EUV development and will install the new system on its Fab 12 GigaFab™ for development of future technology nodes.**

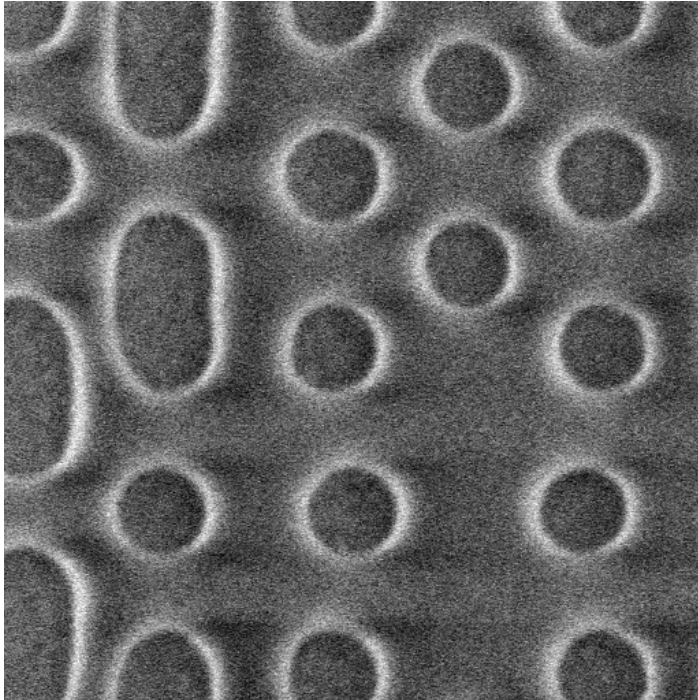
EUVL Process Development

Exposure currently carried out on Alpha Demo Tool (ADT) at IMEC with further processing at TSMC

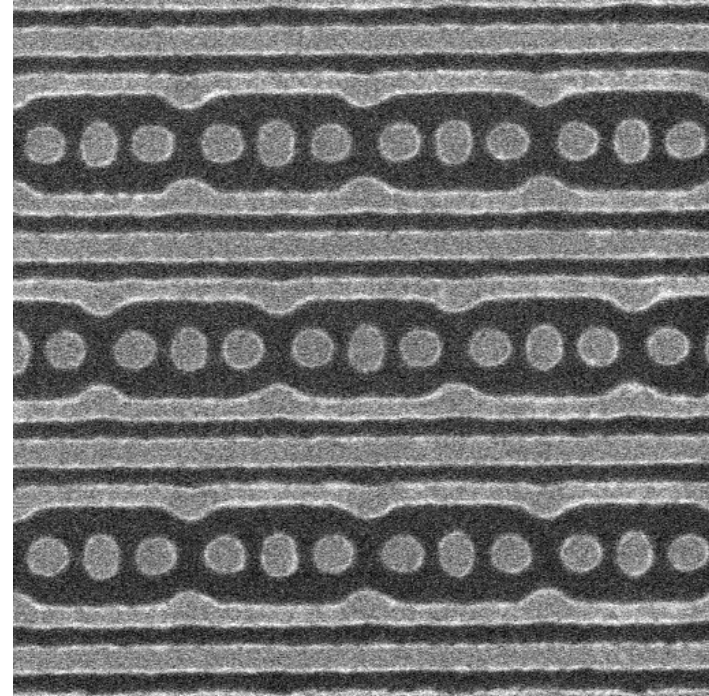


TSMC EUVL Process Development

on Alpha Demo Tool (ADT) at IMEC

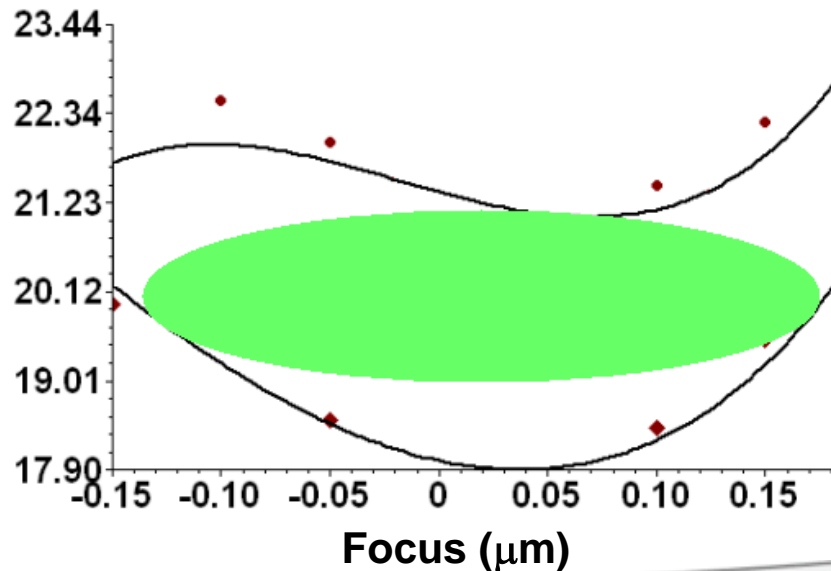
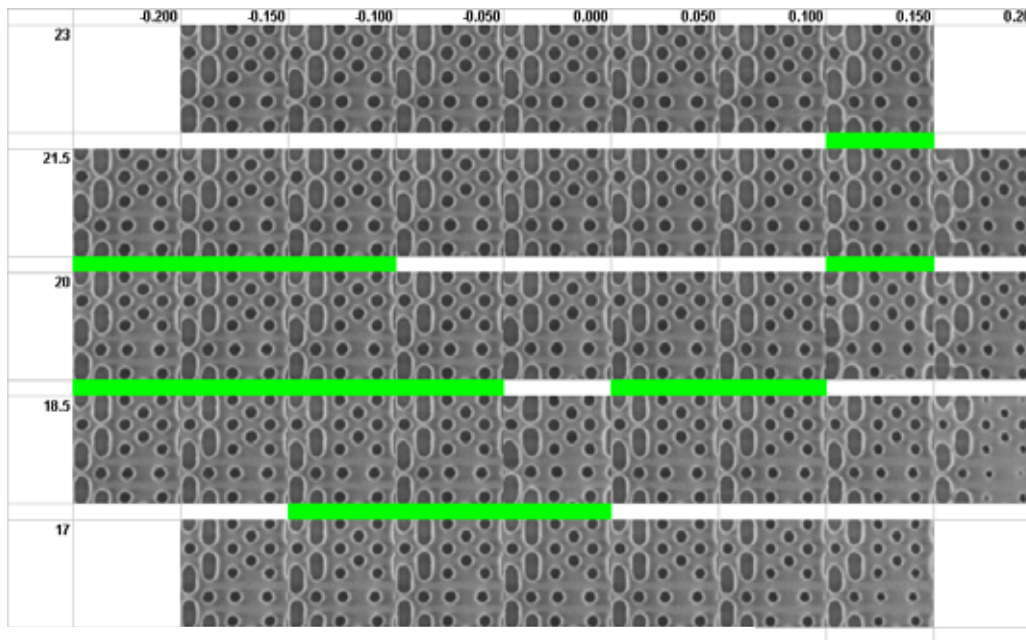


Contact Layer of 32-nm Logic



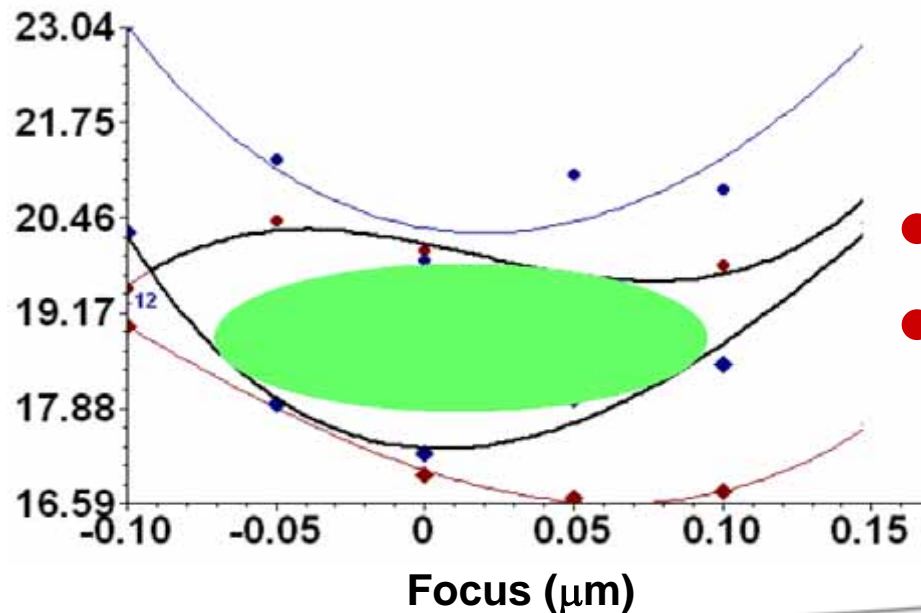
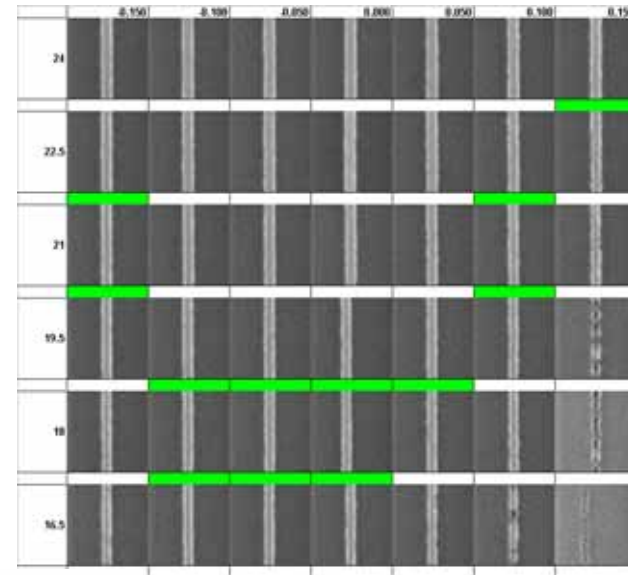
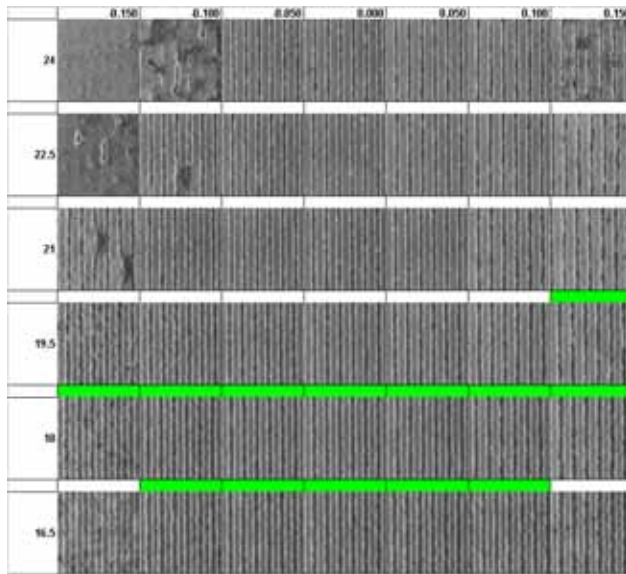
Metal-1 Layer of 20-nm Logic

EUV Process Window for 28-nm Logic



● DOF: $> 0.3 \mu\text{m}$

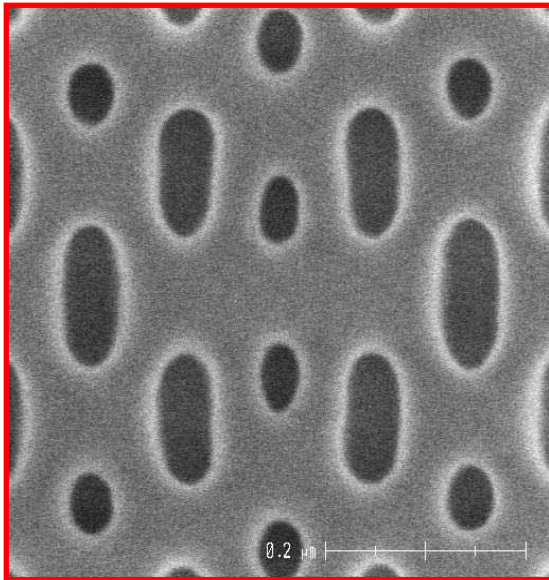
EUV Process Window for 22-nm Logic



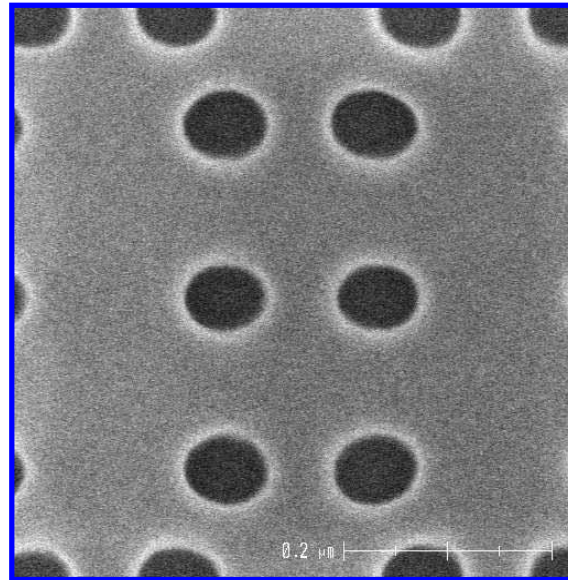
- Common DOF: > 150 nm
- Common EL: ~10%

Example of EUV Resolution Advantage

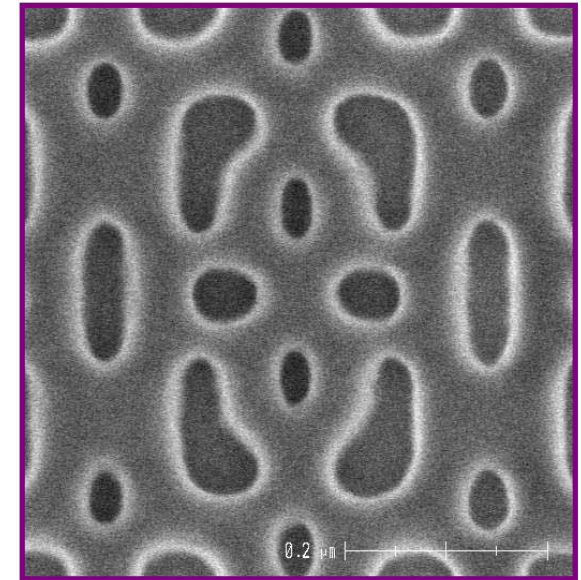
A 22-nm logic layer patterned by single exposure



**EUV exposure of a mask
w/ ½ the pattern**

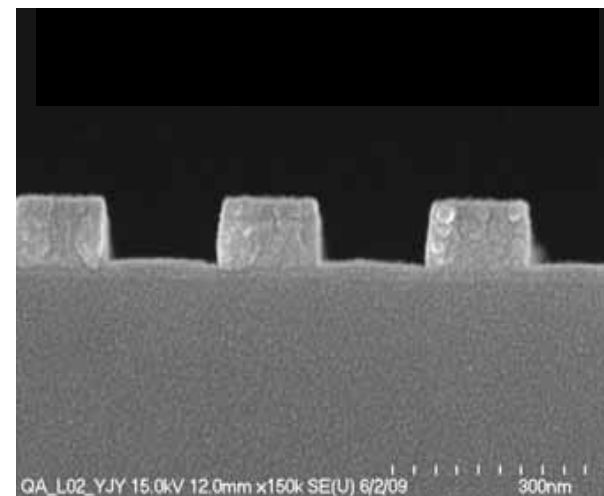
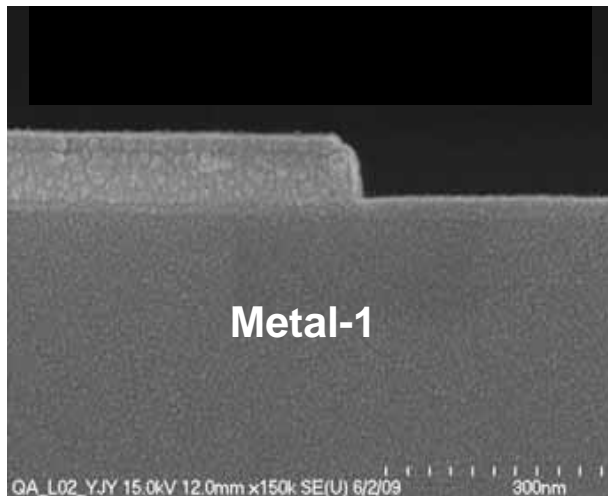
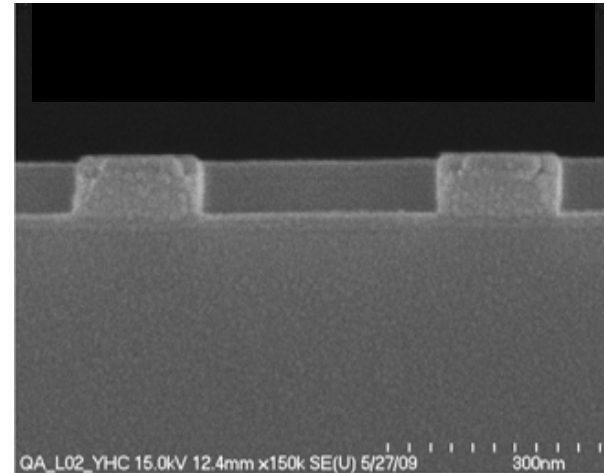
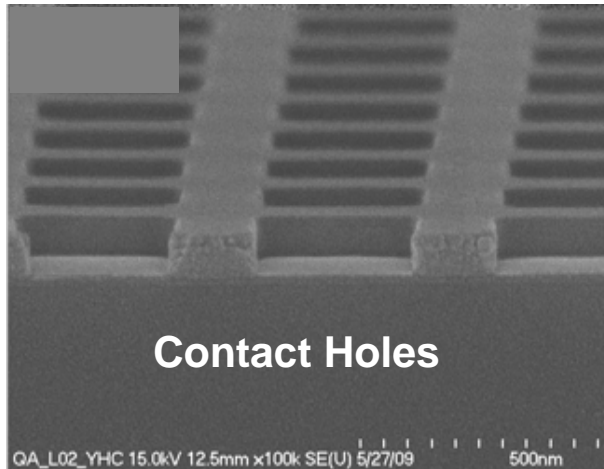


**EUV exposure of a mask
w/ the other ½**

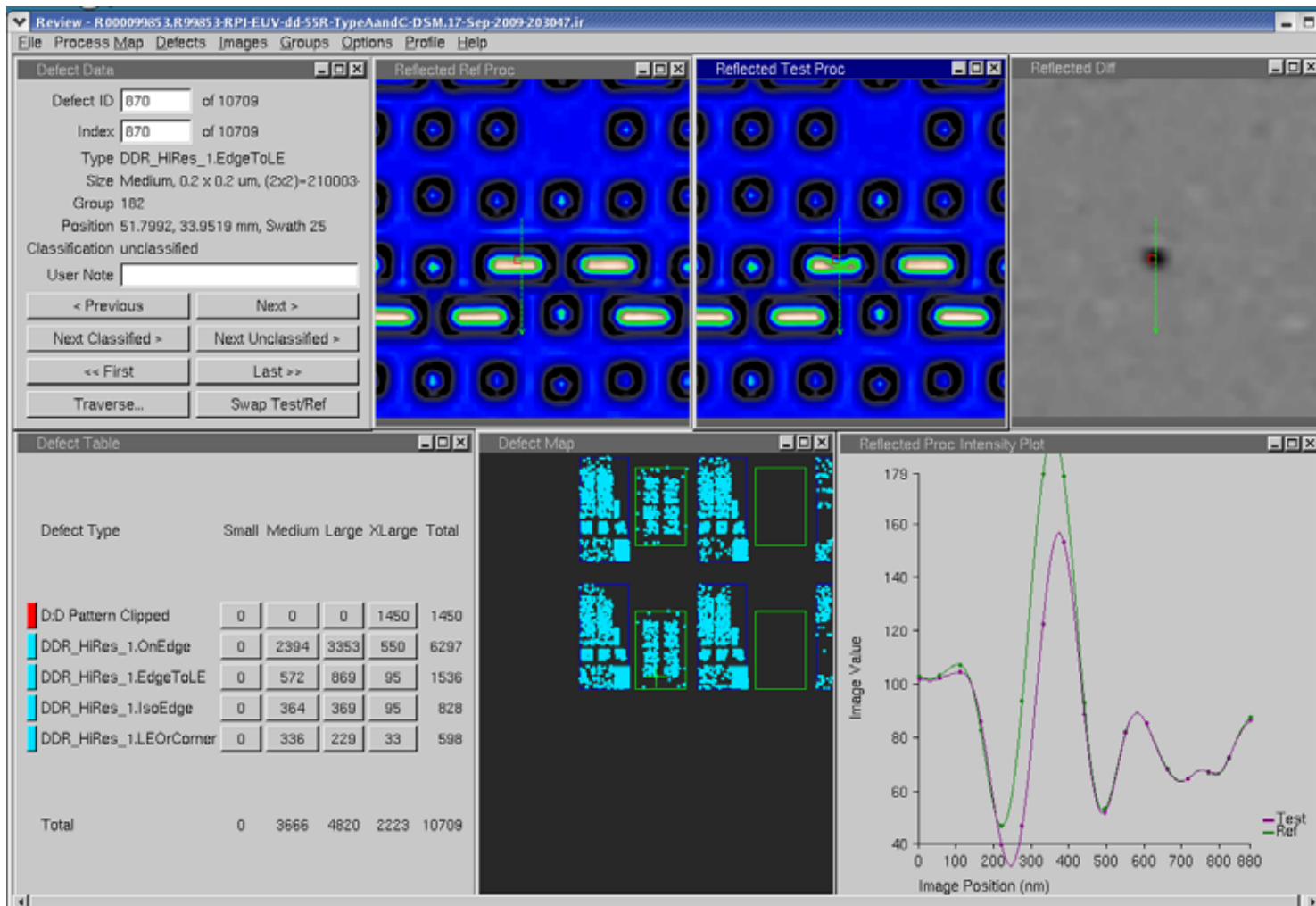


**EUV exposure of a mask
w/ the whole pattern**

In-House Fabrication of EUV Masks

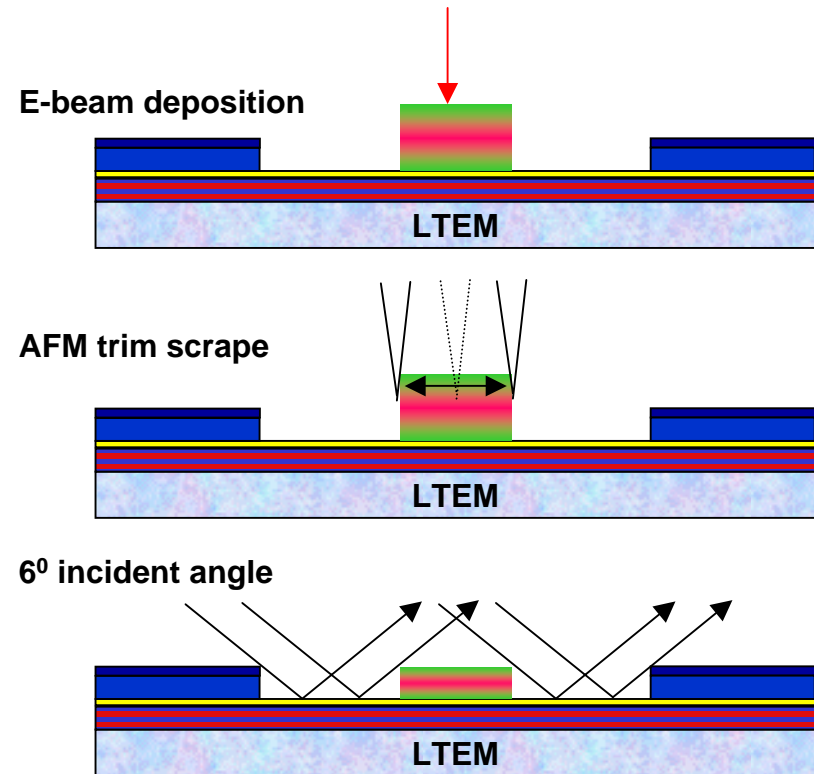
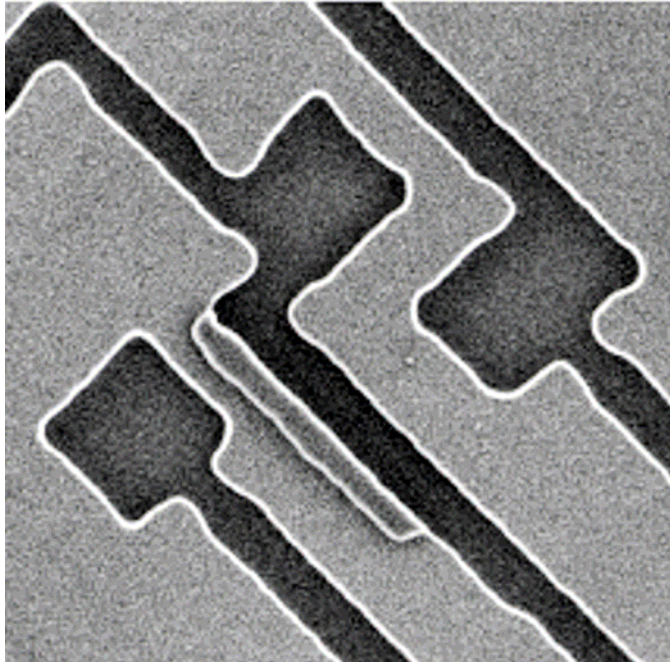


Inspection of Patterned EUV Masks



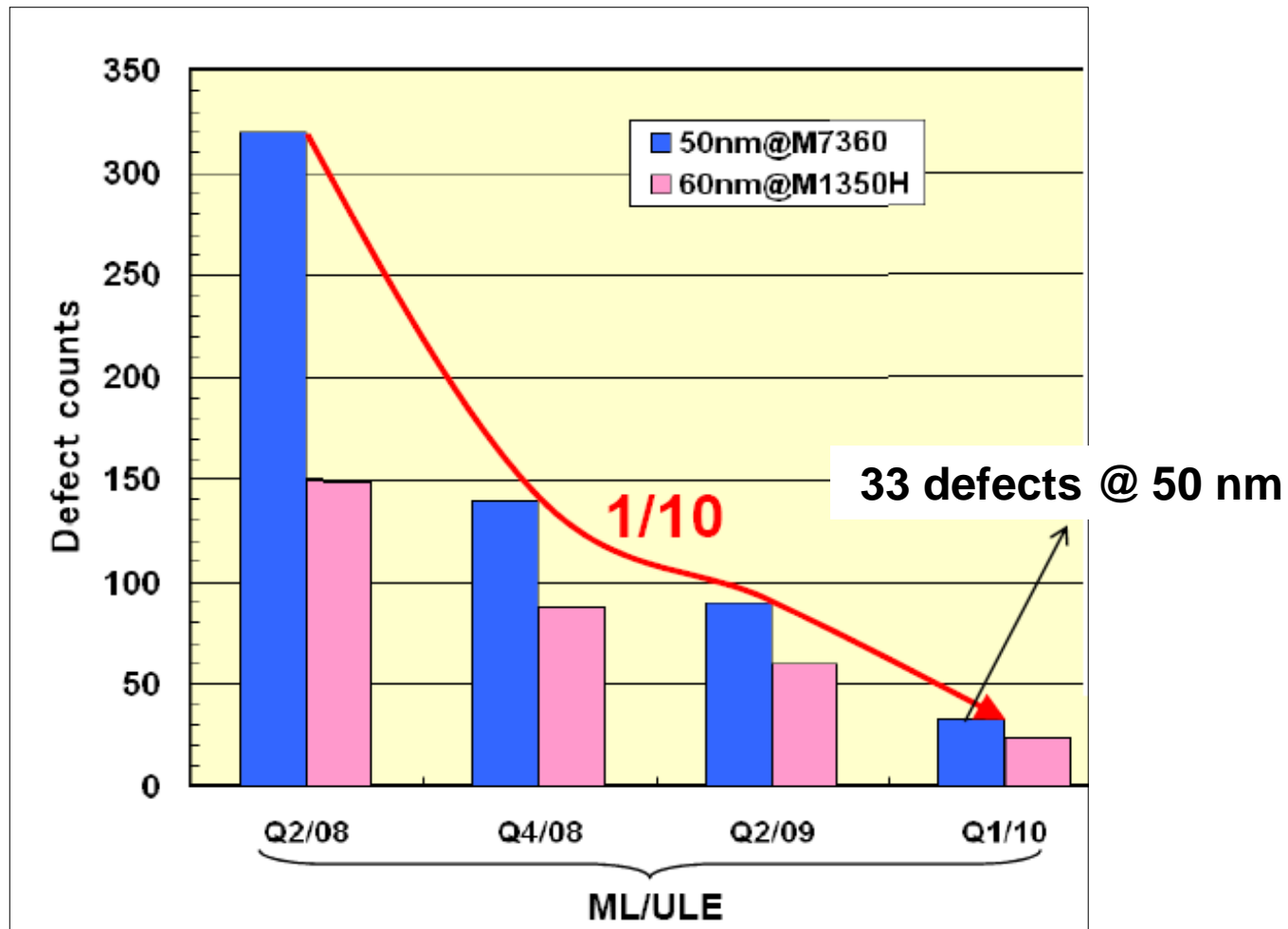
- 22-nm EUV hole mask inspected by a 193-nm-wavelength mask inspection tool

Challenges in EUV Mask Repair



- Need accurate 3-D profile control of deposited area
- Need image verification by actinic AIMS tool

Progress in Mask Blank Defect Reduction



Top 3 Concerns for EUV Lithography

Urgency of Concerns	Technology Component	Mitigation Strategies
1	EUV Source Power	More Sensitive Resists
2	Mask Infrastructure	SEMATECH EMI
3	CA Resist Extensibility	New Resist Chemistries

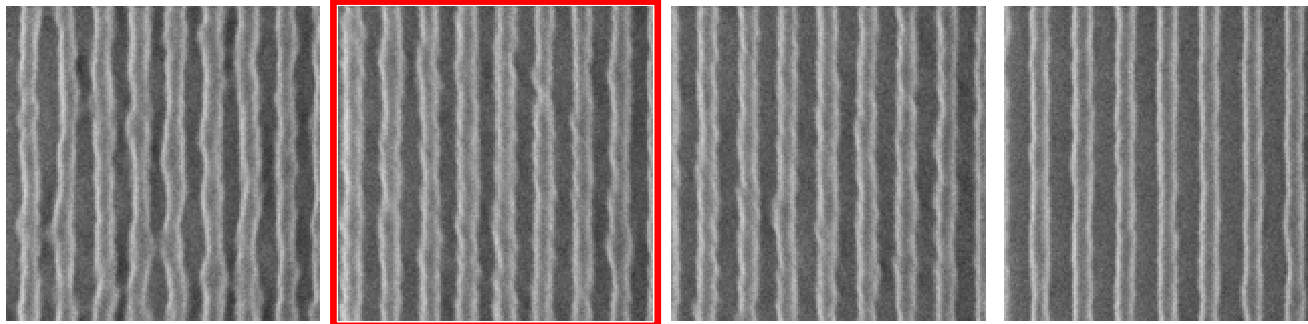
Progress in EUV Resist Sensitivity

Pitch = 52 nm

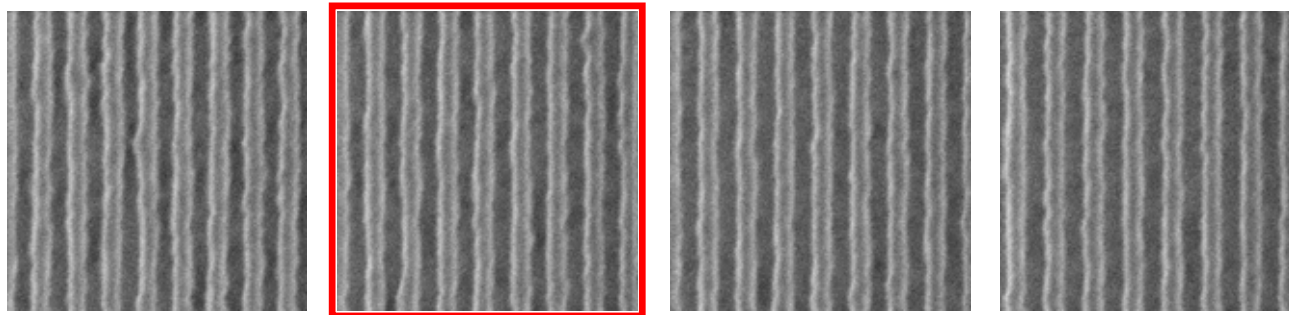
Pitch = 54 nm

Pitch = 56 nm

Pitch = 58 nm



Supplier 1: nominal dose = 8.1 mJ/cm²



Supplier 2: nominal dose = 11.5 mJ/cm²

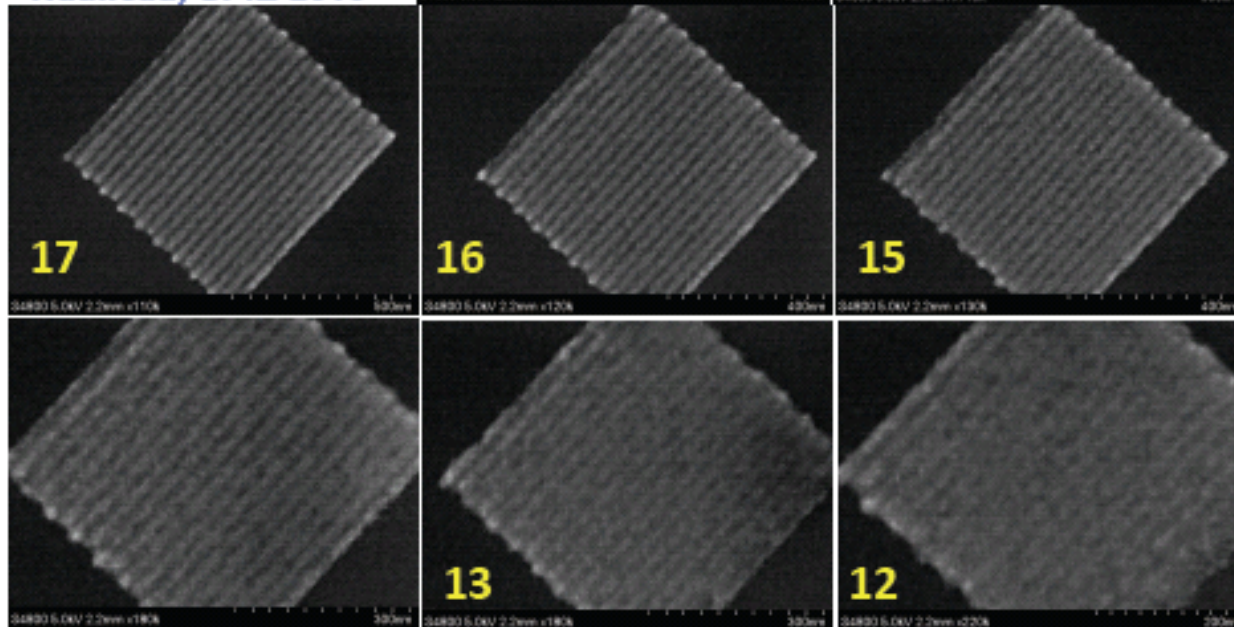
Example of New Resist Chemistry



Inpria XE-31A; LBL eMET dipole, 42 mJ/cm²

Unoptimized, negative-tone resist demonstrates fundamental breakthrough in resolution

Naulleau, SPIE 2010



- Excellent resolution; Expect further sensitivity improvement

EUV Resist-Related JDPs Planned at National Synchrotron Radiation Research Center (NSRRC)

Hsinchu Science Park



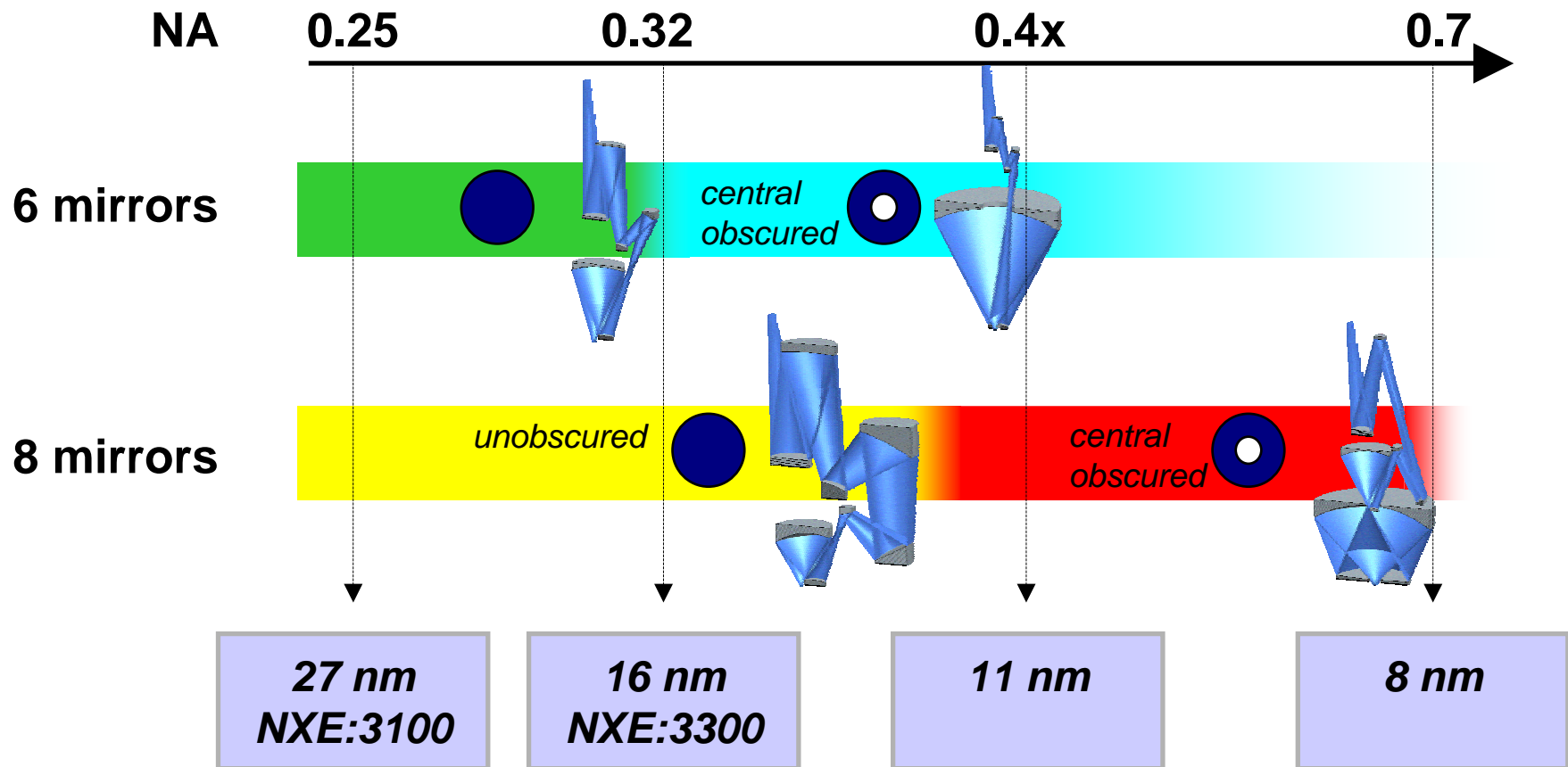
NSRRC

Taiwan Light Source (TLS)
(open to users in 1993)



Designs of High NA EUV Systems

Enabling 11-nm half-pitch and beyond



schematic designs – for illustration only.

W. Kaiser et al., SPIE 2008

Courtesy of Carl Zeiss

Acknowledgement

- **TSMC Nano Patterning Technology Division**
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- **IMEC/ASML**
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